

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	10/707029	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/10/05 12:34
L2	0	"10707029"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/10/05 14:20
L3	270	(deep near3 trench with capacitor) with electrode	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/10/05 15:40
L4	81	3 and (deep near3 trench with capacitor) with node	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/10/05 15:42
L5	62	4 and (deep near3 trench with capacitor) with dielectric	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/10/05 14:23
L6	2	5 and (deep near3 trench with capacitor) with spacer	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/10/05 14:23
L7	1	"6472702".PN.	USPAT; USOCR	OR	ON	2005/10/05 14:32
L8	1	"6255224".PN.	USPAT; USOCR	OR	ON	2005/10/05 14:33
L9	1	"6181014".PN.	USPAT; USOCR	OR	ON	2005/10/05 14:33
L10	1	"5888864".PN.	USPAT; USOCR	OR	ON	2005/10/05 14:34
L11	1	"5198386".PN.	USPAT; USOCR	OR	ON	2005/10/05 14:35
L12	1	"6436760".PN.	USPAT; USOCR	OR	ON	2005/10/05 14:35
L13	1	"6472702".PN.	USPAT; USOCR	OR	ON	2005/10/05 14:35

L14	1710	(trench near3 capacitor) with electrode	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/10/05 15:41
L15	260	14 with oxide	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/10/05 15:42
L16	17	15 with (oxidation oxidizing oxidization)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/10/05 15:44

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<div> <div> L7: (1) "6472702".PN. L8: (1) "6255224".PN. L9: (1) "6181014".PN. L10: (1) "5888864".PN. </div> <div> Search: [] [] [] [] [] DBs: [US:PGPUB] [USPAT] [EPO] [JPO] Default operator: [OR] <input checked="" type="checkbox"/> Details <input checked="" type="checkbox"/> Highlight all the terms initially </div> </div> <div>15 with (oxidation oxidizing oxidization)</div> <div> BPS form ISAR form Image Text HTML </div>									
	U	Document I	Issue Dat	Page	Title	Current O	Current X	Retrieval	Inv
1	r	US 2005018	2005082	32	Semiconductor memory and method of manufacturing the s	365/154			Kito, Ma
2	r	US 2004012	2004070	33	Semiconductor memory and method of manufacturing the s	438/257	257/E21.5		Kito, Ma
3	r	US 2003003	2003021	14	Process for the electrochemical oxidation of a semiconduct	438/770	257/E21.2		Goldbac
4	r	US 6930342	2005081	30	Semiconductor memory and method of manufacturing the s	257/296	438/241;		Kito; Ma
5	r	US 6559069	2003050	13	Process for the electrochemical oxidation of a semiconduct	438/770	257/E21.2		Goldbac
6	r	US 6495411	2002121	14	Technique to improve deep trench capacitance by increasin	438/239	257/301;		Mei; Lei
7	r	US 6306772	2001102	8	Deep trench bottle-shaped etching using Cl2 gas	438/714	257/E21.2		Lin; Mir
8	r	US 6232171	2001051	16	Technique of bottle-shaped deep trench formation	438/246	438/243;		Mei; Lei
9	r	US 6177697	2001012	9	Arrangement for DRAM cell using shallow trench isolation	257/301	257/304;		Cunning
10	r	US 6087214	2000071	9	Arrangement and method for DRAM cell using shallow tre	438/244	257/296;		Cunning
11	r	US 6071823	2000060	8	Deep trench bottle-shaped etch in centura mark II NG	438/714	216/67;		Hung; L
12	r	US 5937292	1999081	10	Nitride cap formation in a DRAM trench capacitor	438/243	257/E21.6		Hammer
13	r	US 5717628	1998021	10	Nitride cap formation in a DRAM trench capacitor	365/149	257/300;		Hammer
14	r	US 5410509	1995042	15	Dynamic type semiconductor memory device with dummy c	365/210	257/E27.0		Morita;
15	r	JP 0619665	1994071	4	SEMICONDUCTOR STORAGE DEVICE		257/68		ISHIGA
16	r	JP 0429807	1992102	16	SEMICONDUCTOR DEVICE AND MANUFACTURE TH		257/303		OZAKI,
17	r	JP 0122746	1989091	3	MANUFACTURE OF SEMICONDUCTOR DEVICE		361/324		IWAMA
<div> <div> File Details HTML </div> </div>									

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